Comparing Executable Specifications regarding Power at Algorithmic Level (ANSI-C/SystemC)

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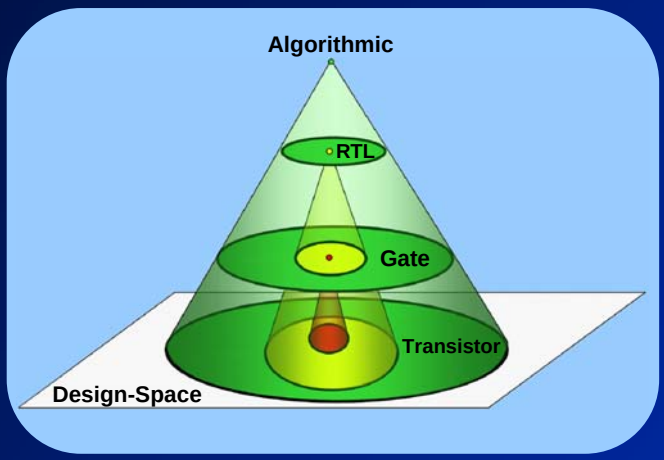
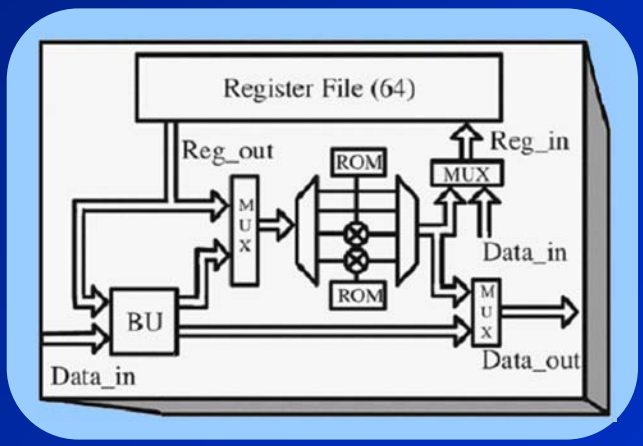
Motivation:

Nanometer scale design comes up with daunting challenges like signal integrity, design for yield and manufacturing or power dissipation. The latter is actually not a new challenge and EDA tools are available that allow for gate- and RT-level power estimation and optimization. For maximum savings, it is mandatory to consider power in the earliest stages of a design flow, since only at highest levels of abstraction, e.g. algorithmic level, the complete design-space is open for exploration and optimization.



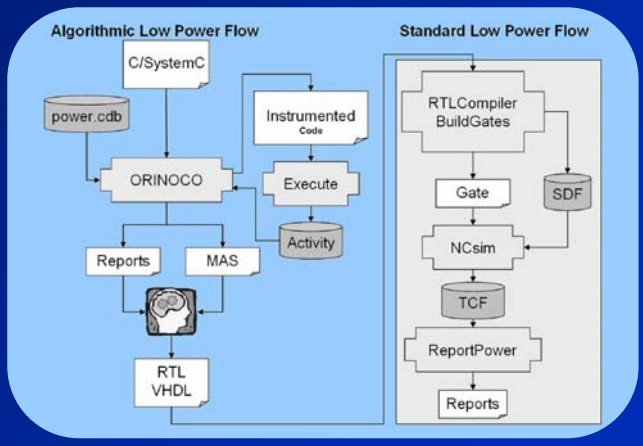
Design Case:

The evaluated benchmark is a 128-point FFT/iFFT processor for ultrawideband communication systems. The proposed mixed-radix multipath delay feedback architecture offers a high throughput rate provided by four parallel data paths. Minimum memory is required by using the delay feedback approach to reorder input data and the intermediate results of each module. Simultaneously, the benchmark was implemented as ANSI-C functions and semantically identical RTL VHDL-components.



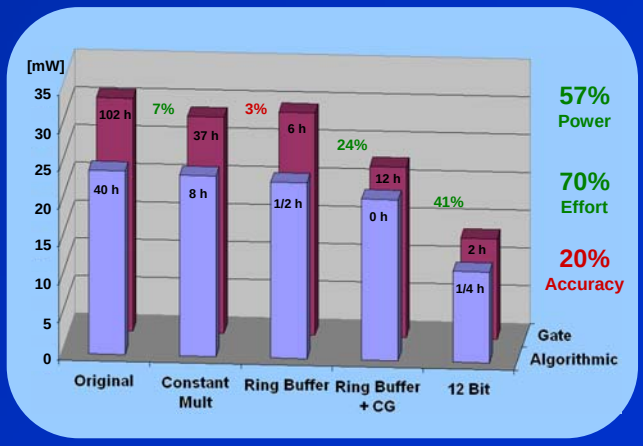
Design Flow:

The concluded 3½ year EU project POET developed design methods for power estimation and optimization. It includes a standard flow extension to make power observable prior to HDL coding. Dataflow activity in C/SystemC models is recorded by automatically inserted trace functions and used to estimate power based on a library of characterized functional units (add, mult, reg, …). Generated reports and micro architecture specifications enable the implementation of power efficient RT code.



Results:

Power dissipation improved by 57%. The overall effort to receive power estimates was reduced by 70% from approx. 160 person hours down to 49. Even though less accurate, the algorithmic level estimates are within reasonable 5 to 21% of the gate-level estimates. Therefore, it is possible to make the right decisions regarding power at algorithmic abstraction level and save significant engineering effort so that the design-space can be explored more extensively leading to improved results.



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