CARL VON OSSIETZKY universität OLDENBURG

Fakultät II *Informatik, Wirtschafts- und Rechtswissenschaften*
Department für Informatik

Internes Kolloquium

Am **Montag, dem 2. Juli 2012,** um **16:15 Uhr** hält

Dipl.-Inform. Kai Hylla
Universität Oldenburg

im Rahmen seiner beabsichtigten Dissertation einen Vortrag mit dem Titel

Creating Virtual System-Level Prototypes for Fast, yet Accurate Power & Timing Estimation of Embedded Hardware

Der Vortrag findet im OFFIS, Escherweg 2, Konferenzsaal F 02 statt.

Zusammenfassung:

During past decades designing embedded hardware drastically changed. In early days designs had a manageable number of RT components and most design steps where performed manually. With progress of customers' demand for more functionality and thus computational power along with Moore's Law, the complexity to cope with also increased. New technologies were developed providing the required performance and coping with the increasing design complexity. Today most designs are developed using platform-based design. A heterogeneous set of modules containing HW, SW, and IP is combined to create the system.
Behaviour of individual HW modules highly depends on the overall system behaviour. From a global point of view the fundamental reason for power dissipation and required execution time is the module's stimulus given by its interaction with the surrounding system. Thus, individual module's power dissipation cannot be estimated without consideration of its environment. But by using today's design flows performing an accurate estimation of large and heterogeneous systems at a low level of abstraction is infeasible.
But such a low-level estimation is required in order to provide power and timing estimates with a sufficient accuracy. Using a low-level characterisation for creating an augmented high-level prototype of the HW module solves this problem. Such prototype can then be embedded into a virtual prototype of the overall system. This virtual system prototype combines augmented HW, SW as well as IP modules. During its execution, the prototype will provide accurate power and timing estimates with respect to the overall system behaviour.
The presentation will introduce an approach for creating fast, yet still accurate virtual prototypes of full-custom hardware modules that are part of a larger and heterogeneous embedded system. Based on a low-level characterisation of the HW modules a high-level prototype is created. Beside the functional behaviour this prototype contains precise information about power and timing. A functional simulation of the overall system prototype allows an estimation of the HW module in terms of power and timing with respect to the overall system behaviour. Up to now, using the presented approach a speed-up of about 87× compared to a conventional RTL estimation is reached.

Betreuer: Prof. Wolfgang Nebel