

Internes Kolloquium

Am Freitag, dem 09. Dezember 2011, um 14:00 Uhr hält

Dipl.-Inform. Eike Thaden
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im Rahmen seiner beabsichtigten Dissertation einen Vortrag mit dem Titel

Semi-Automatic Optimization of Hardware Architectures in Embedded Systems

Der Vortrag findet im OFFIS, Escherweg 2, Konferenzraum F02 statt.

Zusammenfassung:

The development of safety-critical embedded systems requires a well-structured development process starting from initial requirements analysis to hardware/software development to certification and delivery of the final product. Developing products using a rigid process model usually is expensive and time-consuming. Obviously cost and time can be reduced tremendously if some of the comprehensive development process steps do not have to be carried out for the whole system or if they can be avoided completely. For this reason, the development of new products is often based on existing products thus enabling the re-use of as many parts as possible during the development process.

This PhD thesis will contribute a novel methodology for extending safety-critical embedded systems adding additional functionality implemented in software. The proposed methodology focuses on hardware architectures where several subsystems are connected by one global communication bus (FlexRay) each subsystem containing a local communication bus and one or more electronic control units (ECUs). The hereby achieved decoupling of software tasks running on ECUs that are part of different subsystems is exploited by a modular two-tier design space exploration (DSE) process. This process is divided into a global analysis step which assigns new software tasks to subsystems and a local analysis step carried out separately for each subsystem where those tasks are then allocated to ECUs of that subsystem. The DSE process is a semi-automatic optimization process in the sense that engineers guide the DSE process by running it iteratively with successively tightened constraints. A solution produced by the optimization process consists of an allocation of all software tasks to processors of the system and a cost-minimal set of modifications (change processor types and/or add processors) to the system's hardware architecture and has to satisfy all specified constraints.

For both the global and the local analysis step, adequate problem formulations are proposed. An approach for solving the global analysis problem has been developed and evaluated, which is suitable for being encoded using optimal as well as heuristic algorithms. The approach is encoded as SAT modulo theories (SMT) problem for the SMT solver HySAT which is combined with a binary search on the cost variable for calculating optimal solutions. An approach for solving local analysis problems has been developed and evaluated, which uses a pre-analysis step for computing the available capacity on each ECU considering a fixed-priority preemptive scheduler. This new notion of capacity allows to describe local allocation problems by using a set of boolean and linear equalities avoiding the typical fixed-point equation used in schedulability analysis. An implementation based on a state-of-the-art MILP solver has been developed.

Betreuer: Prof. Dr. Werner Damm

Weitere Kolloquiumstermine sind im WWW abrufbar.